Abstract

An oversampling delay is provided between clock and data signals by steering a current between first and second nodes. The first node is coupled to an input differential pair of a clock interpolator and a delayed differential pair of a data interpolator. The second node is coupled to an input differential pair of the data interpolator and a delayed differential pair of the clock interpolator. First clock and data signals are provided to a first data sampling element and, respectively, to the clock and data interpolators. Second clock and data signals, respectively output from the clock and data interpolators, are provided to a second data sampling element. Additional data sampling elements may be linked to form a longer chain of data sampling elements.